WE CLAIM:

1. An embedded computing system, comprising:

a plurality of processors;

a bus coupling to a plurality of peripheral units;

a multiplexor for coupling each of the plurality of processors to the bus in response to an owner signal; and

a set of peripheral-share registers wherein each member of the set includes an entry associated with each of the plurality of peripheral units holding a state value indicating which of the plurality of processors currently owns the associated peripheral unit.

2. The system of claim 1, wherein the multiplexor is bi-directional and comprises:

an address multiplexor coupled to address outputs of each of the plurality of processors wherein the address multiplexor selectively couples one of the processor address outputs to a MUX address output based on the state of the owner signal;

a data multiplexor coupled to data outputs of each of the plurality of processors, wherein the data multiplexor selectively couples one of the processor data outputs to a MUX data output based on the state of the owner signal; and

a shared register having an address port coupled to the MUX address output, a data port coupled to the MUX data output, and a bus port coupled to communicate with the bus.

3. The controller of claim 1, wherein one of the processors is dedicated to executing operating system code and another one of the processors is executing application code.

4. The controller of claim 1 wherein the set of peripheral share registers includes a plurality of request registers such that each request register corresponds to one of the plurality of processors, wherein each request register has an entry associated with each of the peripheral units, and wherein each entry holds a value indicating whether the corresponding processor is requesting ownership of the associated peripheral unit.

5. The controller of claim 1 wherein the set of peripheral share registers includes a plurality of release registers such that each release register corresponds to one of the plurality of processors, wherein each release register has an entry associated with each of the peripheral units, and wherein each entry holds a value indicating whether the corresponding processor is releasing ownership of the associated peripheral unit.

6. The controller of claim 1 wherein the set of peripheral share registers includes a priority register having an entry associated with each of the peripheral units, wherein each entry holds a value indicating which of the plurality of processors wins ownership of the associated peripheral unit when a conflict occurs between two or more of the processors requesting ownership of the associated peripheral unit.

7. The controller of claim 1, wherein the system further comprises the peripheral units and wherein the processors and the peripheral units comprise a single integrated circuit.

8. The controller of claim 1 wherein the state value is dynamically configurable during operation by at least one of the plurality of processors.

9. A method for sharing a plurality of peripheral units in a controller having a plurality of processors comprising:

generating a plurality of access requests using the plurality of processors;

storing a state value associated with each peripheral unit, the state value indicating which of the plurality of processors is a current owner of the associated peripheral; and

selectively coupling each peripheral unit to receive only access requests generated by a particular processor indicated by the state value associated with that peripheral unit.

10. The method of claim 9 further comprising:

dynamically altering the state values to create dynamic ownership associations between a peripheral and the plurality of processors.

11. The method of claim 10 further comprising:

providing a request register for each processor;

providing a release register;

in response to receiving a request for access to a specified peripheral from a first processor, generating an indication in the request register that the first processor has a pending access request;

determining from the state value whether any processor other than the first processor is the current owner of the specified peripheral;

when a second processor owns the peripheral, holding the request in a pending state;

generating an indication in the release register in indicating that the second processor is releasing ownership of the peripheral; and

in response to the indication in the release register, clearing both the request indication and the release indication and changing the state value to indicate that the first processor is the current owner of the specified peripheral.

12. The method of claim 11 wherein the step of providing a request register comprises implementing a data structure for each processor, where each data structure comprises a plurality of entries and each of the entries is associated with a specific one of the plurality of peripheral units.

13. A multiprocessor controller, comprising:

first and second processor cores;

a plurality of peripherals;

a bus coupling the processor cores to the peripherals; and

means for arbitrating between the processor cores for communication access to requested ones of the peripherals, whereby each of the peripherals is only used by one of the core processors at a particular time, wherein the arbitrating means comprises logic for determining which of the processor cores is an owner of a requested one of the peripherals.

14. The controller of claim 13, wherein the bus comprises an address bus and a data bus for each of the processor cores.

15. The controller of claim 14, wherein the arbitrating means further comprises a multiplexor for selecting the address and data busses corresponding to one of the core processors to the bus in response to an owner signal corresponding to the ownership determination.

16. The controller of claim 13, wherein the arbitrating means further comprises a control register for each of the peripherals storing an ownership state indicating which of the core processors controls ownership.

17. The controller of claim 13, wherein the arbitrating means further comprises a multiplexor for selectably coupling the processor cores to the bus in response to an owner signal, the multiplexor comprising:

an address multiplexor coupled to address outputs of the processor cores wherein the address multiplexor selectively couples one of the processor address outputs to a MUX address output based on a state of the owner signal; and

a data multiplexor coupled to data outputs of the processor cores, wherein the data multiplexor selectively couples one of the processor data outputs to a MUX data output based on the state of the owner signal; and

a set of peripheral-share registers wherein a first member of the set includes an entry associated with each of the plurality of peripheral units that holds a state value indicating which of the processor cores currently owns the associated peripheral.

18. The controller of claim 13, wherein the processor cores comprise embedded processor cores integrated on a single integrated circuit chip.

19. The controller of claim 18, further comprising:

a peripheral control register associated with each of the peripheral units, wherein the peripheral control register is shared amongst the plurality of processors and is integrated on the single integrated circuit chip.

20. A multiprocessor computer system, comprising:

a pair of processors;

an input/output bus connected to the processors;

a plurality of peripheral units connected to the input/output bus; and

a multiplexor for selectably coupling each of the processors to the shared input/output, wherein the multiplexor comprises

an address multiplexor coupled to address outputs of each of the processors wherein the address multiplexor selectively couples one of the processor address outputs to a MUX address output; and

a data multiplexor coupled to data outputs of each of the processors, wherein the data multiplexor selectively couples one of the processor data outputs to a MUX data output.

21. The system of claim 20, further comprising:

a set of peripheral registers wherein each member of the set includes an entry associated with each of the plurality of peripheral units that holds a state value indicating which of the processors currently owns the associated peripheral unit.

22. The system of claim 20, wherein the processors comprise embedded processor cores integrated on a single integrated circuit chip.

23. The system of claim 20, wherein the selective coupling performed by the address multiplexor and by the data multiplexor is based on a state of the owner signal.

24. The system of claim 20, wherein the computer system comprises a disk drive controller.

25. A multiprocessor computing system, comprising:

a pair of processors;

a plurality of peripheral units;

a bus coupling to each of the peripheral units; and

a multiplexor selectively coupling each of the plurality of processors to the bus in response to an owner signal, wherein the processors, the peripheral units, and the multiplexor comprise a single integrated circuit.

26. The system of claim 25, further including in the integrated circuit a set of peripheral registers including an entry associated with each of the peripheral units holding a state value indicating which one of the processors owns the associated peripheral unit.

27. The system of claim 26, wherein the state value is dynamically configurable during operation by at least one of the plurality of processors.

28. The system of claim 25, wherein the multiplexor is bi-directional and comprises:

an address multiplexor coupled to address outputs of each of the processors wherein the address multiplexor

selectively couples one of the processor address outputs to a MUX address output based on the state of the owner signal;

a data multiplexor coupled to data outputs of each of the processors, wherein the data multiplexor selectively couples one of the processor data outputs to a MUX data output based on the state of the owner signal; and

a shared register having an address port coupled to the MUX address output, a data port coupled to the MUX data output, and a bus port coupled to communicate with the bus.

29. The controller of claim 28, wherein the set of peripheral share registers includes a plurality of request registers such that each request register corresponds to one of the plurality of processors, wherein each request register has an entry associated with each of the peripheral units, and wherein each entry holds a value indicating whether the corresponding processor is requesting ownership of the associated peripheral unit.

30. The system of claim 25, wherein one of the processors is dedicated to executing operating system code and another one of the processors is executing application code.